IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-30564
	David Hoyle, et al.	Art Unit: 2183
Serial No:	09/703,144	Examiner: Barry J. O'Brien
Filed:	October 31, 2000	Conf. No.: 1032

For: Microprocessor With Branch-Decrement Instruction That Provides a Target and Conditionally Modifies a Test Register if the Register Meets a Condition (Examiner-amended title)

AMENDMENT PURSUANT TO 37 CFR 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION OF FAX TRANSMITTAL
I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on September 14, 2004.

Robin E. Barnum

Dear Sir:

Please amend the specification by inserting before the first line, the following sentence:

--This application claims priority under 35 USC §119(e)(1) of Provisional Application Number 60/183,527, filed February 18, 2000.--

Applicants claimed this priority on Page 1 in Paragraph 1 of the Specification [see COPY of Page 1 of the Spec (paragraph circled) – attached]. However, it was not claimed on the Filing Receipt [see COPY of Page 1 –of the Filing Receipt (item needing revision circled) – attached]. This paragraph was also amended in the first Amendment (Amendment 111), filed January 14, 2004 ([see COPY of Fax Postcard, Page 1 with Fax Mail Certificate and Fax Date, and Page 2 with Paragraph Amendment (3 pages total)].

Please correct this error before issuance of the patent. Since this is obviously an error on the part of the U.S. PTO, no fee is needed.

Respectfully submitted,

Texas Instruments Incorporated
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GF

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/703,144	10/31/2000	2183	710	Ti-30564	7	14	2

23494
TEXAS INSTRUMENTS INCORPORATED
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FILING RECEIPT

"OC000000005739654"

Date Mailed: 02/06/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

David Hoyle, Glendale, AZ ;
Timothy D. Anderson, Dallas, TX ;

Continuing Data as Claimed by Applicant

THIS APPLN CLAIMS BENEFIT OF 60/183,527 2/18/00

Foreign Applications

If Required, Foreign Filing License Granted 02/06/2001

Title

Microprocessor with branch-decrement instruction

Preliminary Class

712

Data entry by : GARNETT, SANDRA **Team :** OIPE **Date:** 02/06/2001

CA

MICROPROCESSOR WITH BRANCH-DECREMENT INSTRUCTION

David Hoyle
Timothy Anderson

This application claims priority under 35 USC §119(e)(1) of Provisional Application No. 60/183,527, filed February 18, 2000 (TI-30302PS)

NOTICE

Technical Field of the Invention

This invention relates to data processing devices, electronic processing and control systems and methods of their manufacture and operation, and particularly relates to microprocessors optimized for digital signal processing.

To: Technology Center: **2183** Total Pages Sent: 19
Facsimile Number: **703-872-9306**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of		TI-30564
	David Hoyle, et al.	Art Unit: 2183
Serial No.:	09/703,144	Examiner: Barry J. O'Brien
Filed:	October 31, 2000	Conf. No.: 1032
For:	Microprocessor With Branch-Decrement Instruction	

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at **703-872-9306** on the date shown below:

Robin E. Barnum _____ January 14, 2004
Robin E. Barnum Date

FACSIMILE COVER SHEET COPY

X	FACSIMILE COVER SHEET	X	AMENDMENT 111 (17 Pages)
___	NEW APPLICATION	X	EOT (1) month (1 Page)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL (# Pages)
___	ASSIGNMENT (# Pages)	___	APPEAL (# Pages)
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	REPLY BRIEF (IN TRIPLICATE) (# Pages)
___	CONTINUATION APP'N (# Pages)	___	
___	DIVISIONAL APP'N		

NAME OF INVENTOR(S): David Hoyle, et al.	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/703,144** **Filing Date:** October 31, 2000
TITLE OF INVENTION: Microprocessor With Branch-Decrement Instruction	
TI FILE NO.: **TI-30564** / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 1/14/04 DUE: 12/16/03 ATTY/SEC'Y: RDM/reb	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hoyle et al
Serial No.: 09/703,144
Filed: October 31, 2000
For: MICROPROCESSOR WITH BRANCH-DECREMENT INSTRUCTION

Art Unit: 2183
Examiner: Barry J. O'Brien
Docket: TI-30564

AMENDMENT UNDER 37 C.F.R. 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION OF FAX TRANSMITTAL UNDER 37 C.F.R. §1.6(b)

I hereby certify that the above correspondence is being facsimile transmitted to the Patent and Trademark Office on **January 14, 2004.**

Robin E. Barnum

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated September 16, 2003. A petition and fee for a one month extension of time is attached. These amendments are respectfully submitted as a full and complete response to that Action.

Please amend the above referenced application as follows:

In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 9 to 10 as follows:

--This application claims priority under 35 USC §119(e)(1) of Provisional Application No. 60/183,527, filed February 18, 2000 ~~(TI-30302PS)~~.--

Rewrite the paragraph at page 6, line 16 to page 8, line 6 as follows:

--In microprocessor 1 there are shown a central processing unit (CPU) 10, data memory 22, program memory 23, peripherals 60 and an external memory interface (EMIF) with a direct memory access (DMA) 61. CPU 10 further has an instruction fetch/decode unit 10a-c , a plurality of execution units, including an arithmetic and load/store unit D1, a multiplier M1, an ALU/shifter unit S1, an arithmetic logic unit ("ALU") L1, a shared multi-port register file 20a from which data are read and to which data are written. Decoded instructions are provided from the instruction fetch/decode unit 10a-c to the functional units D1, M1, S1, and L1 over various sets of control lines which are not shown. Data are provided to/from the register file 20a from/to to load/store ~~units~~ unit D1 over a first set of busses 32a, to multiplier M1 over a second set of busses 34a, to ALU/shifter unit S1 over a third set of busses 36a and to ALU L1 over a fourth set of busses 38a. Data are provided to/from the memory 22 from/to the load/store ~~units~~ unit D1 via a fifth set of busses 40a. Note that the entire data path described above is duplicated with register file 20b and execution units D2, M2, S2, and L2. Load/store unit D2 similarly interfaces with memory 22 via a set of busses 40b. In this embodiment of the present invention, two unrelated aligned double word (64 bits) load/store transfers can be made in parallel between CPU 10 and